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Overview of Wireless Clock Routing Design For VLSI Layouts

Rajine Swetha R.[1] *and* ***Sumithra Devi K. A.***[2]

[1] *ECE research centre, R. V. College of Engineering, Bangalore, India*
E-mail: rajineswethar@gmail.com
[2] *MCA Department, R. V. College of Engineering, Bangalore, India*
E-Mail: sumithraka@gmail.com

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Summary
The matured area of antenna theory and design in communication field is evolved to support various communication applications of the modern wireless era. This field gains its importance by its innate ability to seamlessly integrate with different domain areas. VLSI is a promising area of the future electronic applications, where miniaturization is the base rule. All electronic systems operate with a system clock frequency and each circuit block in the board generates its independent internal clock if necessary for the operation of the logical blocks. In this paper the design possibility of using a multibeam forming antenna for transmitting the common system clock frequency throughout the PCB is explored. The proposed design increases the chip performance by reducing inter circuitry delays and has the potential to maximize the chip performance in multifold times by its optimized intra chip, inter chip clock routing.

Key words: *Wireless clock routing, application of antennas in PCB, area optimizing by wireless routing.*

1. INTRODUCTION

The field of antennas is one of the pioneering and promising fields of communication. The field is grown rapidly with the period of time and has found its way through its integration with many other instruments whose transmitted signals are critically important for mankind. With the advent of RADARS the communication between the antennas, positioned apart became easier. This development of the wireless communication has shrunk the area of EARTH as such. VLSI circuits undergo the seven stages of the physical design. The last stage is optimization and design compaction. Recent research is focused on area compaction of the chip under consideration, as in many industrial applications; there is an immediate need for compactness, so that power and area for operation is less. In this paper antennas are proposed to be used for communication between the chips. This approach eliminates the need for wired clock routing.

2. MOTIVATION

Clock routing is a critical step in the physical design of any VLSI circuit. Many optimized designs encounter failure at the stage of "Routing". The major reasons for many of such failures are: (i)The wire congestion between the circuits in the chip (Local Routing) and between the chips on the board (Global Routing); (ii)The nearness of power lines and clock lines, generating a strong interference from the power lines affecting the clock frequency navigating the chip; (iii)While designing care is to be taken that there should be always an 30% leeway to accommodate the routing stage in the given chip area; (iv)Clock delays should be reduced to a minimum in High Speed Circuits. These factors lead to an insatiable need for a wireless design for the purpose of clock routing. This need is the primary objective for the design proposed in this paper.

3. LITERATURE SURVEY

The work published by Moore et.al has the description of a wireless test technique for the testing of very large scale IC's and wafers [1]. Further in the development of antennas; adaptive array antennas and multiple antennas together called as Smart Antennas solve the problems faced by the multipath wave propagation [2].Another recent research conducted by Batra et.al focuses on investigating a novel technique for coping with the strong mutual coupling imposed in the electrically small antenna arrays using Eigen mode reception and digital beam forming. From these papers the design for the wireless communication between chips on a board is conceived. VLSI circuits are prone to clock delays, congestions which are the major areas of research work.

4. TRADITIONAL ROUTING IN CHIP

Rapid growth in VLSI technology has increased the number of transistors that fit on a single chip to about two billion. A frequent problem in the design of such high performance and high density VLSI layouts is that of routing wires that connect such large numbers of components. Most wire routing problems are computationally hard [14]. The quality of any routing algorithm is judged by the extent to which routing constraints and design objectives are satisfied. The design objectives include minimizing total routed wire length, minimizing total capacitance induced in the chip, reducing clock delays. The Figure 1, shows the congestion in a part of the board circuit.

5. SMART ANTENNA FUNCTIONS

Smart antennas are array of antennas with smart signal processing algorithms used to identify a spatial signal quantity such as direction of arrival and use it to form the beam vectors to track the source of generation. The antenna could optionally be any sensor [3]. Smart antenna techniques are currently used in acoustic signal processing, in cellular applications like W-CDMA. Smart antennas have two main functions: DOA (direction of arrival) estimation and Beam forming [4]. There are various options available for beamforming. They include the DSP chip based implicit method and chip legacy method and the antenna based beamforming option [10]. There are various beamforming methods. A comparison of different methods are shown in the Table 1.

From the comparison in the Table 1, we see that the antenna based beamforming technique is more suited for the VLSI chip communication, as the interference rejection is high and the gain is high compared to chip implicit and chip legacy methods. The following Figure 2 and 3, give the structure of antenna transmission and reception and the radiation pattern of the adaptive antenna used in wireless communication.

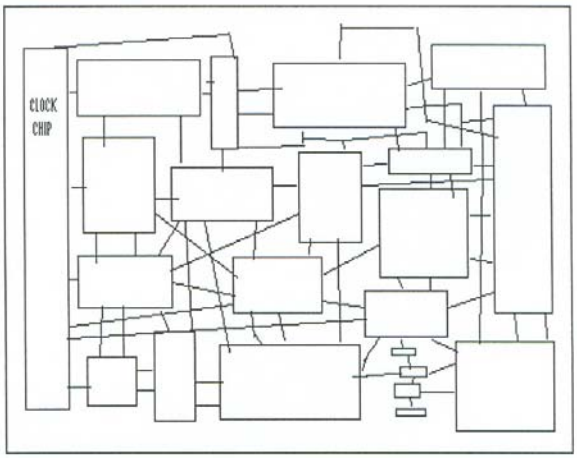

Figure 1. Typical wire congestion in a chip

Table 1. Various methods of Beamforming

CHIP-LEGACY	CHIP-IMPLICIT/EXPLICIT	ANTENNA-BASED
802.11a/g	802.11n	802.11a/g/n
DSP based	DSP based	Additive to 802.11 at Physical layer
Doesn't use every client	Optional 802.11n	Feedback built into feedback client support
Provides upto 1-2db gain	Provides upto 3db gain	Provides upto 9db gain
Can't focus energy	Can't focus energy	Focuses RF energy to target
Interference Present	Interference present	Up to -17dB interference rejection

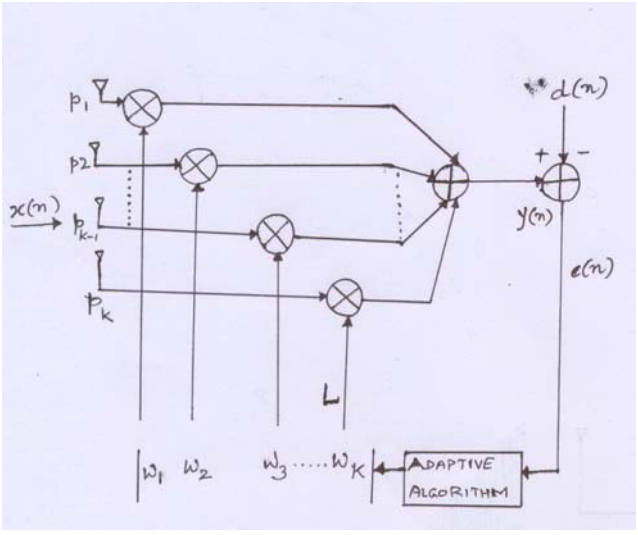

Figure 2. Structure of adaptive beamforming antenna

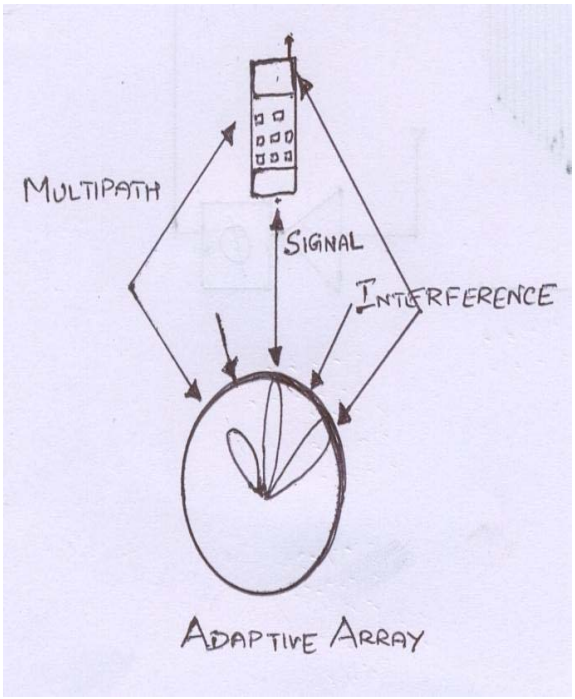

Figure 3. Beam formation for adaptive array antenna system

6. PROPOSED DESIGN

In VLSI circuits initially the placement step is completed based on partitioning stage. The optimization algorithm is applied to the design. When the stage of routing comes, it's viewed as local routing and global routing.

The clock routing is taken into consideration in this paper. The system clock is generated by the crystal oscillator in the board. This frequency is digitized. In local routing the concentration is focused on the inside chip routing [7]. Here the beam forming antennas can be used for the

reception of the system clock signals. The received signals can then be used as input to the further circuitry on the board.

In the global routing the Antenna is placed in the centre of the board and then the system clock frequencies are fed for transmission to the various chips on the board [8].These frequencies are received by the targeted receiving antennas located in each chip and further transmitted to the individuals in the chip [13,15]. These transmitted and received antenna signals are received by the transreceivers located in each chip. Thus similar to the cellular networking in communication systems, an on board wireless clock routing communication system can be envisioned.

The antenna beamforming can be modeled according to the following principle described.

If, L signals in angles {o1;o2; :::;oL} impinge on a uniform linear array with M elements, the received signal at the m th element at time instant ' t' can be written as

$$X\,m(t) = X_{Li=1} si(t)\, e^{jkd}\, \sin(oi) + n(t) \qquad (1)$$

where k denotes the wave number and n(t) denotes the noise at that time instant. Same equation can be represented in vector form as

$$X(t) = AS(t) + N(t) \qquad (2)$$

for
$X(t) = [\ x1(t)\ x2(t)\ :::\ xM(t)\ ]T$
$S(t) = [\ s1(t)\ s2(t)\ :::\ sM(t)\ ]T$
$N(t) = [\ n1(t)\ n2(t)\ :::\ nM(t)\ ]T$

where S(t) denotes the signals impinging on the array elements, N(t) denotes the noise received by the elements and A is the steering matrix, whose columns are the array response vectors for a signal impinging from o_i direction, given by:

$A = [\ a(o1)\ a(o2)\ :::\ a(oL)\ ]T$

where $a(oL) = e^{jkd \sin oL}$

In adaptive arrays, complex weights are applied to the element outputs given by:

$$W = [\ w_1\ w_2\ :::\ w_M\ ]^T \qquad (4)$$

Then the array output can be written as:

$$Y(t) = M\, X_{l=1} X_l(t)\, w_o\, l = WmX(t) \qquad (5)$$

Thus using the output of the array elements in the antenna the direction of the beam formed can be precisely transmitted according to the design requirements of the circuit and the targeted implementation of the digitized system clock can be made to propagate to the predefined circuits in the chip.

Internal to the chip the clock can be converted by an appropriate DAC design to analog signals that can be integrated with the analog and mixed mode circuits, high speed circuits. The use of beamforming antennas also ensures that the signals can be transmitted to the chips which are identified as the targets [11]. The radiation pattern of the antenna array is formed by adding the signal phases. At the same time chip which don't require transmitted input will be out of the pattern generated.

The Figure 4 shows the typical multiple antenna tranceiver beamforming employing beamforming antenna implementation for maximum gain and power combing. The direction of the beam is shown by the radiation pattern of the antenna expressed as the major lobe. The transmission and the reception of the signal and the consideration of the beam formation angles are clearly shown in the Figure 4.

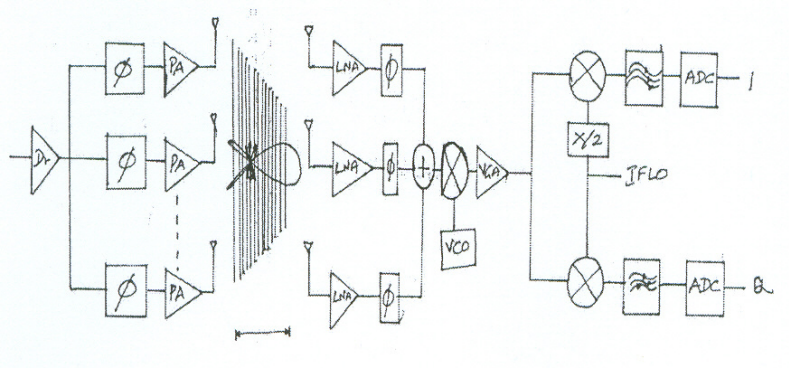

Figure 4. Beamforming implementation

7. EXPECTED RESULTS

The wireless clock routing consideration proposed in this paper serves to address the prime purpose of reducing the frequency interferences sourcing from the adjoining power and clock lines in the chip layout design considerations. The validated trans-receiver designs available for use ensure the precise transmission and reception of the clock frequency throughout the chip area under consideration.

The circuit at the consecutive stage, is activated from the standby mode just as the antenna tunes to the clock frequency The clock routing congestions on the board are reduced by antenna tuning at the inter and intra circuit levels. This design consideration further ensures that the delay reduction in the clock transmission inside the chip as compared to its conventionally clock routed counterpart.

8. CONCLUSION AND FUTURE SCOPE

The design discussed in this work is focused to the current day necessity of miniaturization of the chip area. This opens a new integration of fields which will occupy the center stage of the modern wearable electronic applications.

By wireless global routing clock strategy the wastage in the board floor area and the necessity of the clock transmission through the vias in the different layers of the layout design are eliminated. This approach to clock routing further provides the designer, the freedom of placement of the computational blocks according to the design optimization; thereby increasing the overall chip performance.

This approach of wireless clock routing can be extended in the future to the input signal transmissions; in designs where the intermediate output generated out of a single chip is to be given to multiple components on the board; bringing about an new generation of chip layout designs where concept of wired clock routing congestions, interdependent clock and power routing constraints are obsolete.

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